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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/678,142	10/03/2000	Noriaki Sakamoto	10417-049001	6940

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EXAMINER	
NORRIS, JEREMY C	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 06/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/678,142	SAKAMOTO ET AL.	
	Examiner	Art Unit	
	Jeremy C. Norris	2841	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4-18,20-26,32-40,42-46,48-50,52-55,57-59 and 61-75* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4,5,7,10-15,17,20-26,32-37,39,42-44,48,52,53,57,61,63 and 65-75* is/are rejected.

7)☒ Claim(s) *6,8,9,16,18,19,38,40,41,45,46,49,50,54,55,58,59,62 and 64* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 December 2002* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/29/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 4, 5, 7, 10, 11-15, 17, 20-26, 32-37, 39, 42-44, 48, 52, 53, 57, 61, 63, and 65-75 are rejected under 35 U.S.C. 102(b) as being anticipated by US 5,221,428 (Ohsawa).

Ohsawa discloses a sheet-like board member (2) comprising: a first planar surface; a second planar surface disposed opposite to the first surface, said second planar surface having a semiconductor element mount region (8) defined thereon; and a mask (9) disposed on the second planar surface and having a pattern corresponding to a plurality of first pads formed in or in the vicinity of the semiconductor element mount region, said mask comprising a conductive film, and guide holes (6) into which guide pins are inserted (10) [claim 10], further comprising: a wiring disposed on said second planar surface (see fig. 2B) [claim 4], wherein the first pads are bonding pads or pads on which solder balls are to be fixed [claim 5] wherein the conductive coating film is disposed on the second planar surface to form a passive element die pad and/or outer lead electrode [claim 7], wherein the sheet-like board member is formed from a conductive foil, and the conductive film is formed of a material different from that of the

conductive foil (col. 3, lines 20-50) [claim 11], Including a wiring continuously extending from a land (fig. 2B) [claim 65, 70] wherein the sheet-like board is made of metal [claim 69].

Similarly, Ohsawa discloses, a sheet-like board member (2) comprising: a first planar surface; a second planar surface disposed opposite to the first planar surface; a protuberance formed on said second planar surface; and guide holes (6) into which guide pins are inserted, wherein the protuberance comprises a plurality of first pads (8) in or in the vicinity of a semiconductor element mount region defined on the second planar surface [claim 12], wherein the protuberance comprises wirings (figure 2B) integrally formed with the first pads [claim 13], wherein the protuberance comprises second pads integrally formed with the wirings [claim 14], wherein the first pads comprise bonding pads, or pads on which solder balls or bumps are mounted [claim 15] wherein the protuberance comprises passive element die pads and/or outer lead electrodes [claim 17], comprising protuberances arranged in a plurality of patterns as a unit, wherein the unit is arranged in a matrix pattern on the sheet-like board member (fig. 2B) [claim 20], wherein the sheet-like board member comprises mainly Cu, Al, an Fe-Ni alloy, a Cu-Ai multi-layered member, or an Al-Cu-Al multi-layered member (col. 3, lines 20-30) [claim 21], comprising a conductive coating film formed of material different from that of the protuberance and formed on an upper surface of the protuberance (col. 4, lines 1-10) [claim 22], wherein a side surface of the protuberance has an anchoring structure [claim 23], further comprising: a conductive film comprising an anvil-shaped structure in the vicinity of a top surface of the protuberance (fig. 1E) [claim 24],

comprising a conductive film on the protuberance, wherein the conductive film comprises Ni, Au, Ag or Pd (col. 4, lines 1-15) [claim 25]. Including a wiring continuously extending from a land (fig. 2B) [claim 67, 72] wherein the sheet-like board is made of metal [claim 71].

Additionally, Ohsawa, discloses, a sheet-like board member (2) comprising: a planar surface; a sheet-like front side of predetermined thickness which is provided on the planar surface; a plurality of first pads (8) formed in or in the vicinity of a semiconductor element mount region defined on the planar surface; protuberances formed on said planar surface and include wirings (fig. 2B) integrally formed with the first pads, said plurality of first pads and said protuberances formed within an abutting region defined on said planar surface and guide holes (6) into which guide pins are inserted. Examiner notes that the limitation "said abutting region provided to contact with an upper metal mold" [claim 26] is an intended use limitation and is thus only considered to the extent that the limitation impacts the claimed structure. Thus a prior art meeting all the other claimed structural limitations only needs to be capable of being used in the claimed manner. Also, Ohsawa discloses, wherein said planar surface having the protuberances, some of which semiconductor elements are disposed thereon, are all encapsulated in plastic (5a) [claim 32], the wiring extending continuously form the first pad [claim 73]

Moreover Ohsawa discloses a sheet-like board member (2) comprising: a first planar surface a second planar surface disposed opposite to the first surface, said second planar surface having a semiconductor element mount region defined thereon;

and a mask (9 or alternately 5a) for etching disposed on the second planar surface and having a pattern corresponding to a plurality of first pads (8) formed in or in the vicinity of the semiconductor element mount region and guide holes into which guide pins are inserted [claim 33], wherein the mask comprises a photoresist (5a) [claim 34], wherein the mask comprises a conductive film (9) [claim 35], further comprising: a wiring (fig. 2B) disposed on said second planar surface, wherein the mask is formed on a region corresponding to the wiring integrally connected to one or more of the first pads [claim 36], wherein the first pads are bonding pads or pads on which solder balls are to be fixed (fig. 2B) [claim 37], wherein the conductive coating film is disposed on the second planar surface to form a passive element die pad and/or outer lead electrode [claim 39], wherein the sheet-like board member comprises a pressed metal (col. 3, lines 10-45) [claim 42], wherein the sheet-like board member is formed from a conductive foil, and the conductive film is formed of a material different from that of the conductive foil (col. 3, lines 10-45) [claim 43], wherein the sheet-like board is partially etched in an area not covered by the mask (fig. 1E) [claim 44], wherein the sheet-like board is partially etched in an area not covered by the conductive film (fig. 1E) [claim 48], comprising a conductive film formed on the protuberance (see col. 4, lines 1-15) [claim 52], wherein an Ag plating is formed on the protuberance (col. 4, lines 15-25) [claim 53], wherein the sheet-like board is partially etched in area not covered by the mask, [claim 57], Including a wiring continuously extending from a land (fig. 2B) [claim 68, 75] wherein the sheet-like board is made of metal [claim 74].

Furthermore Ohsawa discloses, a method of manufacturing a semiconductor device comprising: preparing a sheet-like board member (2) as defined in any one of claims 10, 12, 26, 33 and 44-60 (see above); partially etching the second planar surface of the sheet-like member so as to form the first pads (8); disposing a circuit element onto a portion on the sheet-like board member; molding a surface of the sheet-like board member by an insulating resin (5a) so that the sheet- like board member is covered [claim 61].

Moreover, Ohsawa discloses, a method of manufacturing a semiconductor device comprising: preparing a sheet-like board member (2) as defined in any one of claims 12 and 26 (see above); disposing a circuit element onto a portion of the protuberances of the sheet-like board member; molding a surface of the sheet-like board member by an insulating plastic (5a) so that the sheet-like board member is covered [claim 63], including a wiring (fig. 2B) continuously extended from a land [claim 65-68].

Allowable Subject Matter

Claims 6, 8, 9, 16, 18, 19, 38, 40, 41, 45, 46, 49, 50, 54, 55, 58, 59, 62, and 64 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Claims 8, 18, 40 state the limitation "wherein a passive element to be placed on the passive element die pad comprises a chip resistor or a chip capacitor". This

limitation, in conjunction with the other claimed limitations was neither found to be disclosed in, nor suggested by the prior art. Claims 9, 19, 41 state the limitation "wherein patterns which are substantially identical with guide pins or guide holes into which the guide pins are inserted are formed in mutually-opposing side of the sheet-like board member". This limitation, in conjunction with the other claimed limitations was neither found to be disclosed in, nor suggested by the prior art. Claims 45, 46, 49 50, 54, 55, 58, 59 state the limitation "wherein a positioning mark is provided on the sheet-like board member". This limitation, in conjunction with the other claimed limitations was neither found to be disclosed in, nor suggested by the prior art. Claims 47, 51, 56, 60 state the limitation "wherein a guiding hole is formed with the sheet-like board member". This limitation, in conjunction with the other claimed limitations was neither found to be disclosed in, nor suggested by the prior art. Claims 62, 64 state the limitation "wherein the sheet-like board member is fixed by means of vacuum suction". Claims 6 16, and 38 state the limitation "wherein the conductive coating is disposed in the semiconductor element mount region to form a die pad". This limitation, in conjunction with the other claimed features, was neither found to be disclosed in nor suggested by the prior art.

Response to Arguments

Applicant's arguments with respect to claims 4, 5, 7, 10, 11-15, 17, 20-26, 32-37, 39, 42-44, 48, 52, 53, 57, 61, 63, and 65-75 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremy C. Norris whose telephone number is 571-272-1932. The examiner can normally be reached on Monday - Friday, 9:30 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JCSN

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